REMARKS

Claims 4, 21 and 22 are amended and, claims 1, 2, 24 and 27 are canceled. Claims 4-23, 25, 26 and 28-38 are now active in this application. No new matter has been added.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 103 IN FINAL OFFICIAL ACTION OF JULY 11, 2003

I. Claims 1, 4, 6, 7, 11, 15, 16, 20, 25 and 26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. (U.S. Patent No. 6,157,072) in view of Takasaki et al. (U.S. Patent No. 4,980,736), Kobayashi et al. (U.S. Patent No. 6,476,867; hereinafter Kobayashi) and Sugawa (U.S. Patent No. 5,869,850).

The rejection is moot as to independent claim 1, canceled by this amendment.

In the Official Action of July 3, 2002, original claim 4, depending from claim 1 via claim 2, was objected to, but the Examiner indicated claim 4 would be allowable if rewritten in independent form including all the limitations of the base claim (1) and any intervening claims (2). The Amendment dated September 30, 2002 amended claim 4 to be in independent form including all the limitations of base claim 1, but not dependent claim 2. The present amendment to claim 4 now adds the limitation of original claim 2, and claim 1 is canceled. Claim 8 is amended to depend from claim 4. Consequently, amended independent claim 4 is believed to be allowable as are claims 8, 9-12, 15 and 28 depending from amended claim 4.

Claims 7, 25 and 26 are amended to delineate that "an energy level at an interface between said amorphous silicon nitride layer and said amorphous silicon layer is discontinued on a valance band side and equal on a conduction band side."

II. Claims 2, 5, 17, 18, 23 and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al. and Sugawa as applied to claims 1, 4, 6, 7, 25 and 26 and further in view of Deane et al. (U.S. Patent No. 6,064,091).

The rejection is moot as to canceled claims 2 and 24.

III. Claims 8-10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al. and Sugawa, as applied to claims 1 and 4 above, and further in view of Anagnostopoulos (U.S. Patent No. 5,563,404), Ota (U.S. Patent No. 4,496,981) and Waki et al. (JP 01-311511).

IV. Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al. and Sugawa, as applied to claim 4, and further in view of Fukuda et al. (U.S. Patent No. 5,635,327).

V. Claims 13, 14 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kozuka et al. (JP 09-102627), and Kobayashi et al.

VI. Claims 21 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al.

The present amendments to claims 21 and 22 add the limitation that "the carrier generation/multiplication layer is composed of an amorphous silicon carbide of the p-type conductivity to inhibit injection of electrons into the carrier generation/multiplication layer" and "an energy level at an interface between said amorphous silicon nitride layer and said amorphous silicon layer is discontinued on a valance band side and equal on a conduction band side."

VII. Claims 27-30, 33, 37 and 38 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kobayashi et al. and Sugawa, as applied to claims 1, 4, 6, 7, 16, 25 and 26 above, and further in view of Kodama et al. (USPN 5,122,431).

The rejection is moot as to canceled claim 27.

VIII. Claims 31, 32 and 34 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., Kozuka et al. and Kobayashi et al., as applied to claims 13, 14 and 19 above, and further in view of Kodama et al.

IX. Claims 35 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama et al. in view of Takasaki et al., as applied to claims 21 and 22 above, and further in view of Kodama et al.

X. As noted in the response dated November 10, 2003, the present invention generally relates to a layered structure of a photoelectric conversion device. More specifically, as recited in each of the independent claims, the photoelectric conversion device essentially comprises I-a-Si layer sandwiched by p-a-SiC layer and n-a-SiN.

The Examiner relies upon Nakayama as showing a SiN layer, and refers to the paragraph at column 20, lines 34-46 of this reference, which describes:

> In the practice of the present invention, ***the semiconductor layer*** is not limited to a PIN-type amorphous silicon semiconductor image sensor. Thus, it ***may be any*** of PIN, NIP, NI, PN, MIS, heterojunction, homojuction, Schottky-barrier and ***mixed type sensors fabricated by using amorphous or microcrystalline silicon semiconductors which include***, among others, amorphous silicon a--Si, hydrogenated amorphous silicon a--Si:H, hydrogenated amorphous silicon carbide a--SiC:H, ***amorphous silicon nitride***, etc., and alloys of silicon with carbon or any of germanium, tin and other metals. Aside from the above, the linear image sensor to which the invention is applicable includes those using other semiconductors such as GaAs, GdS and other types of semiconductors.

Clearly, in this paragraph, usable examples as the semiconductor, as a whole, are listed and a-SiN is merely introduced as one example therefor, but is **NOT** as an example for the specific layer of n-type a-SiN. Thus, there is no teaching in this reference regarding the specific combination of layers of p-type a-SiC, a-Si, and n-type a-SiN (the carrier generation/multiplication layer provided between the p-type a-SiC electron injection inhibiting layer and the n-type a-SiN hole injection inhibiting layer), as recited in the present claims.

In the Advisory Action dated December 19, 2003, the Examiner maintains that "As noted in Nakayama et al. (column 3, lines 17-20 and column 4, lines 58-59), any of these semiconductor materials can be interchanged."

However, column 3, lines 15-21 of Nakayama et al. describe:

> ...By the provision of this resin film, the boards 102 of individual linear image sensors 106 are prevented from entrapment by the rotary cutter 105 of the dicer or falling down to break.
>
> For this cutting of the glass substrate board 102 with the dicer, there must be a cutting margin A, which is generally at least 0.2 mm, as shown in FIG. 21.

In addition, column 4, line 58 through column 5, line 8 of Nakayama et al. describes:

> The image sensor of the present invention, as a solution to the first problem mentioned above, generally comprises an insulating substrate board and, as formed one-dimensionally on said substrate board, a plurality of blocks each consisting of a plurality of photodiodes, the corresponding number of blocking diodes respectively connected in series and opposite polarity to said photoelectrodes, and a common electrode connected to said number of said blocking diodes in common, with a matrix wiring interconnecting the photodiodes in the same relative positions within respective said blocks, characterized in that said photodiodes and blocking diodes formed one-dimensionally on said insulating substrate board is covered with a transparent interlayer insulating film and each of said photodiodes is connected to the corresponding blocking diode in series and opposite polarity by a coupling electrode through a contact hole formed in said transparent interlayer insulating film (FIG. 1).

As is readily seen from the sections referred to by the Examiner, there is absolutely nothing about "any of these semiconductor materials can be interchanged", let alone any teaching or suggestion regarding the specific combination of layers of p-type a-SiC, a-Si, and n-type a-SiN (the a-Si carrier generation/multiplication layer provided between the p-type a-SiC electron injection inhibiting layer and the n-type a-SiN hole injection inhibiting layer), as recited in the present claims.

As to Takahashi et al., Kobayash et al., Sugawa, Deaane et al., Anagnostophulos, Ota, Waki et al., Fukuda et al. and Kozuka et al., none of these references disclose or suggest the deficiency of Nakayama et al., identified above. Therefore, even if the

teachings of Takahashi et al., Kobayash et al., Sugawa, Deaane et al., Anagnostophulos, Ota, Waki et al., Fukuda et al. and Kozuka et al. were somehow combined with the disclosure of Nakayama et al., the claimed invention does not result.

As noted in the previous response also, regarding the Examiner using Sugawa as a prior art teaching of the claimed limitation regarding energy levels by referring to Figures 6 and 7 of this reference, Applicants point out once again that, contrary to the Examiner's finding, Figures 6 and 7 do **NOT** teach the claimed limitation regarding energy levels at the interface of the specific type layers recited in the claims.

As to Deane et al., even tough it relates to a large image sensor does not evince with certainty that such sensor is a photoconversion device. Thus, as noted in the previous response, Deane et al. does not relate to photoelectric conversion device and does not disclose a sandwich structure. Therefore, this reference is not relevant to the claimed invention.

As to the rejection of claims 21 and 22 in section **VI** above, the Examiner admits that Nakayama et al. does not disclose the inhibiting layer on only a substrate. However, the Examiner maintains that Takasaki et al. further teaches the inhibiting layer (Fig. 1A, #15) on only a substrate (Fig. 1A, #16). Thus, the Examiner contends it would have been obvious to a person of ordinary skill in the art to have the inhibiting layer on only a substrate of Takasaki et al. with the device of Nakayama et al., since one would be motivated to place the inhibiting layer on something like a substrate for support, as implied from Fig. 1A of Takasaki et al.

In the previous response, Applicants noted that in Fig. 1A of Takasaki et al., blocking layer 15 is formed **ON** electrode 16 which is formed **ON** substrate 11. In the

Advisory Action, the Examiner maintains that Takasaki et al. does tache the blocking layer on a substrate. However, Fig. 1A of Takasaki et al. clearly evinces that blocking layer 15 is formed **OVER** substrate 11 and **ON** electrode 16. In the semiconductor art, it is well understood by an antisan that when a layer is **ON** another layer, there is **contact** between the layers. There is not contact between blocking layer 15 and substrate 11. Cleary, blocking layer 15 is formed **ON** electrode 16 and **OVER** substrate 11.

The structural arrangement in Fig. 1A of Takasaki et al. is the same structural arrangement shown in Fig. 3 of Nakayama et al. Thus, there is no realistic motivation for an artisan to modify the device of Nakayama et al. in view of the teaching of Takasaki et al., as this results in the exactly the same structural arrangement already disclosed in Nakayama et al.

XI. In view of the above, claims 4-23, 25, 26 and 28-38, as amended, are patentable over Nakayama et al., Takahashi et al., Kobayash et al., Sugawa, Deaane et al, Anagnostophulos, Ota, Waki et al., Fukuda et al. and Kozuka et al. and Kodama et al., considered alone or in combination. Therefore, the allowance of claims 4-23, 25, 26 and 28-38, as amended, is respectfully solicited.

CONCLUSION

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that

might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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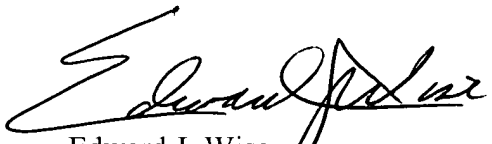

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